IN THE CLAIMS:

1. (Currently Amended) A semiconductor device, comprising:

a bulk substrate and an active layer;

an isolation structure formed in said active layer, said isolation structure defining an area;

a multiple thickness buried oxide layer formed between said bulk substrate and said active layer, said multiple thickness buried oxide layer having a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate;

said active layer being formed above said multiple thickness buried oxide layer, said semiconductor device being formed in said active layer above said multiple thickness buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer, said doped back gate region extending under an entirety of said multiple thickness buried oxide layer ~~between~~ and the area defined by said isolation structure.

2. (Original) The device of claim 1, wherein said bulk substrate is comprised of silicon.

3. (Original) The device of claim 1, wherein said semiconductor device is a transistor.

4. (Original) The device of claim 1, wherein said semiconductor device is part of at least one of a microprocessor, a memory device and a logic device.

5. (Original) The device of claim 1, wherein said active layer is comprised of silicon.

6. (Original) The device of claim 1, wherein said active layer has a thickness ranging from approximately 5-30 nm.

7. (Original) The device of claim 1, wherein said buried oxide layer is comprised of silicon dioxide.

8. (Original) The device of claim 1, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

9. (Original) The device of claim 1, wherein said semiconductor device is a transistor having a channel region, at least a portion of said channel region being positioned above a section of said buried oxide layer that has a thickness that is less than a thickness of a remaining portion of said buried oxide layer.

10. (Original) The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being at least partially positioned under said gate electrode.

11. (Original) The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being substantially aligned with said gate electrode.

12. (Original) The device of claim 8, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

13. (Currently Amended) A transistor, comprising:

a bulk substrate and an active layer;

an isolation structure formed in said active layer, said isolation structure defining an area;

a buried oxide layer formed between said bulk substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said

active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer being formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer, said doped back gate region extending under an entirety of said buried oxide layer ~~between~~ and the area defined by said isolation structure.

14. (Previously Presented) The transistor of claim 13, wherein said bulk substrate is comprised of silicon.

15. (Previously Presented) The transistor of claim 13, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

16. (Previously Presented) The transistor of claim 13, wherein said active layer is comprised of silicon.

17. (Previously Presented) The transistor of claim 13, wherein said active layer has a thickness ranging from approximately 5-30 nm.

18. (Previously Presented) The transistor of claim 13, wherein said buried oxide layer is comprised of silicon dioxide.

19. (Previously Presented) The transistor of claim 13, wherein said transistor comprises a channel region, at least a portion of said channel region being positioned above at least a portion of said first section of said buried oxide layer.

20. (Previously Presented) The transistor of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

21. (Previously Presented) The transistor of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

22. (Previously Presented) The transistor of claim 13, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

23. (Currently Amended) A transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate and an active layer;

an isolation structure formed in said active layer, said isolation structure defining an area;

a buried oxide layer formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer being formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer, said doped back gate region extending under an entirety of said buried oxide layer ~~between~~ and the area defined by said isolation structure.

24. (Previously Presented) The transistor of claim 23, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

25. (Previously Presented) The transistor of claim 23, wherein said active layer is comprised of silicon.

26. (Previously Presented) The transistor of claim 23, wherein said active layer has a thickness ranging from approximately 5-30 nm.

27. (Previously Presented) The transistor of claim 23, wherein said buried oxide layer is comprised of silicon dioxide.

28. (Previously Presented) The transistor of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

29. (Previously Presented) The transistor of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried gate oxide layer is substantially aligned said gate electrode.

30. (Previously Presented) The transistor of claim 23, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

31.-55. (Canceled)

56. (Currently Amended) A semiconductor device, comprising:

a bulk substrate and an active layer, said active layer being doped with a first type of dopant material;

a multiple thickness buried oxide layer formed between said bulk substrate and said active layer, said multiple thickness buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate;

said active layer being formed above said multiple thickness buried oxide layer, said semiconductor device being formed in said active layer above said multiple thickness buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer, said doped back gate region being a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

57. (Previously Presented) The device of claim 56, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

58. (Currently Amended) A transistor, comprising:

a bulk substrate and an active layer, said active layer being doped with a first type of dopant material;

a buried oxide layer formed between said bulk substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer, said doped back gate region being a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

59. (Previously Presented) The transistor of claim 58, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

60. (Currently Amended) A transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate and an active layer, said active layer being doped with a first type of dopant material;

a buried oxide layer formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer; and

a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer, said doped back gate region being a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

61. (Previously Presented) The transistor of claim 60, wherein said transistor further comprises a gate electrode and wherein said first section of said buried gate oxide layer is substantially aligned said gate electrode.

62.-73. (Canceled)

74. (Currently Amended) The device of claim 1, wherein said active layer comprises a first type of dopant material and said doped back gate region ~~being~~ is a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

75. (Currently Amended) The transistor of claim 13, wherein said active layer comprises a first type of dopant material and said doped back gate region ~~being~~ is a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

76. (Currently Amended) The transistor of claim 23, wherein said active layer comprises a first type of dopant material and said doped back gate region ~~being~~ is a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

77. (Currently Amended) The device of claim 56, wherein said doped back gate region extends beneath an entirety of said multiple thickness buried oxide layer ~~within~~ and an area defined by an isolation structure formed in the active layer.

78. (Currently Amended) The transistor of claim 58, wherein said doped back gate region extends beneath an entirety of said buried oxide layer ~~within~~ and an area defined by an isolation structure formed in the active layer.

79. (Currently Amended) The transistor of claim 60, wherein said doped back gate region extends beneath an entirety of said buried oxide layer ~~within~~ and an area defined by an isolation structure formed in the active layer.